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PTO/SB/08A (08-00)

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	TO BE ASSIGNED
Filing Date	HEREWITH
First Named Inventor	Peters, Michael J.
Group Art Unit	
Examiner Name	
Attorney Docket Number	00939s-050510US

10/099154
03/14/02

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
Be	AA	4,821,173		Young, et al.	4/1989	
I	AB	5,168,937		Blecha, Jr.	11/1992	
	AC	5,438,591		Ginetti et al.	6/1995	
Be	AD	5,572,437		Rostoker et al.	11/1998	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
Be	AE	JP	4273382			2/1993		

Examiner Signature

Heath Lawrence

Date Considered

5/31/05

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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	
		Filing Date	
		First Named Inventor	Peters, Michael J.
		Group Art Unit	
		Examiner Name	
Sheet 2 of 2	Attorney Docket Number	00939s-050510US	

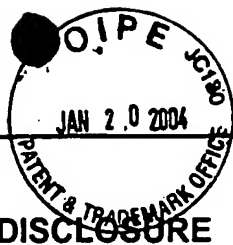
OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
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AL	AF	IBM Technical Disclosure Bulletin; Vol. 30, No. 4; September 1987; Testing Multiple Discrete Software Components by Connecting Real and Simulated Hardware Components; pp 1844,455	
I	AG	An Emulator for CMOS ASICS; VLSI Systems Design; May 1987; pp. 8	
I	AH	1990 IEEE International Symposium on Circuits and Systems, May 1,1990; P. Agrawal et al; "Can Logic Simulators Handle Bidirectionality and Change Sharing?"; pp. 411-414	
AL	AI	IEEE Design & Test of Computers; vol. 7, no. 3, June 1990; Coelho; "A VHDL Standard Package for Logic Modeling"; pp. 25-32	

Examiner Signature	<i>Mark Savere</i>	Date Considered	5/31/05
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PTO/SB/08A (08-03)

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	1	of	2
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Complete if Known

Application Number	10/099,754
Filing Date	March 14, 2002
First Named Inventor	Peters, Michael J.
Art Unit	3661
Examiner Name	Not yet known
Attorney Docket Number	00939s-050510US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
De	A1	US-4488354		12-18-1984	Chan et al.	
	A2	US-4683384		07-28-1987	Shibata et al.	
	A3	US-4744084		05-10-1988	Beck et al.	
	A4	US-4791357		12-13-1988	Hyduke	
	A5	US-4942317		07-17-1990	Tanaka et al.	
	A6	US-4978633		12-18-1990	Seefeldt et al.	
	A7	US-4980889		12-25-1990	DeGuise et al.	
	A8	US-5105373		04-14-1992	Rumsey et al.	
	A9	US-5300835		04-05-1994	Assar et al.	
	A10	US-5317698		05-31-1994	Chan	
	A11	US-5406147		04-11-1995	Coyle et al.	
	A12	US-5426591		06-20-1995	Ginetti et al.	
	A13	US-5426739		06-20-1995	Lin et al.	
	A14	US-5428750		06-27-1995	Hsieh et al.	
	A15	US-5452229		09-19-1995	Shankar et al.	
	A16	US-5479123		12-26-1995	Gist et al.	
	A17	US-5481484		01-02-1996	Ogawa et al.	
De	A18	US-5535223		07-09-1996	Horstmann et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
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PTO/SB/08B (08-03)

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete If Known		
			Application Number	10/099,754	
			Filing Date	March 14, 2002	
			First Named Inventor	Peters, Michael J.	
			Art Unit	3661	
			Examiner Name	Not yet known	
Sheet	2	of	2	Attorney Docket Number	00939s-050510US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>De</i>	C1	Agrawal, P. et al; "Can Logic Simulators Handle Bidirectionality and Charge Sharing?"; 1990 IEEE international Symposium on Circuits and Systems, May 1, 1990; pp. 411-414.	
	C2	Beresford, Roderic "An Emulator for CMOS ASICS"; VLSI Systems Design; May 4, 1987; pp. 8.	
	C3	Chranowska-Jeske, M. et al. "Improved I/O pad assignment for sea-of-gates placement algorithm", IEEE, Aug. 1992.	
	C4	Coelho; "A VHDL Standard Package for Logic Modeling"; IEEE Design & Test of Computers; vol. 7, No. 3, Jun. 1990; pp. 25-32.	
	C5	IBM Technical Disclosure Bulletin; Testing Multiple Discrete Software Components by Connecting Real and Simulated Hardware Components; pp. 1844,455, Vol. 30, No. 4; Sep., 1987.	
<i>De</i>	C6	Nolan, Joe & Salt, Tom "The integration of power supply components within standard cell integrated circuits", IEEE, May 1989, p.13-5.1-5.4	

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